

40V N-Channel Power SpeedFET

• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• Application

- BLDC Motor driver
- DC-DC
- Load Switch

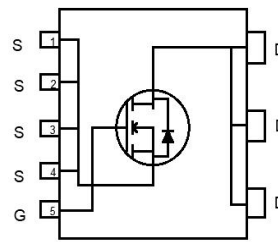
• Ordering Information:

Part NO.	ZMSA006N04HSR
Marking	ZMS006N04H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2000

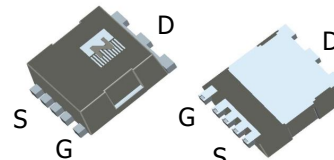
• Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage ^①	V_{GS}		±20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	340	A
	I_D	$T_C=75^\circ\text{C}$	292	A
	I_D	$T_C=100^\circ\text{C}$	253	A
Pulsed Drain Current ^①	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	1020	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	214	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.0	W
Operating Junction Temperature	T_J		-55 to +175	°C
Storage Temperature	T_{STG}		-55 to +175	°C
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	360	mJ
		$L=0.3\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	756	mJ
ESD Level (HBM)	CLASS 2			

• Product Summary



$V_{DS} = 40\text{V}$
 $R_{DS(ON)} = 0.6\text{m}\Omega$
 $I_D = 340\text{A}$



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•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.7	°C/W
Thermal resistance, junction-ambient	R_{thJA} ②		-	50	°C/W
Soldering temperature	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	2.8	4.0	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=40V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=30A$		0.6	0.8	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=10A$		60		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=30A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	6900	-	μF
Output capacitance	C_{oss}		-	2100	-	
Reverse transfer capacitance	C_{rss}		-	86	-	
Gate Resistance	R_g	$f=1MHz$	-	1.4		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=20A, V_{GS}=10V$	-	94	-	nC
Gate - Source charge	Q_{gs}		-	21	-	
Gate - Drain charge	Q_{gd}		-	26	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	39	-	ns
Turn-ON Rise time	t_r		-	42	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	31	-	ns
Turn-Off Fall time	t_f		-	12	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, di_S/dt=$	-	72	-	ns
Reverse Recovery Charge	Q_{RR}	$100A/\mu s, I_S=50A$	-	85	-	nC

Fig.1 Gate-Charge Characteristics

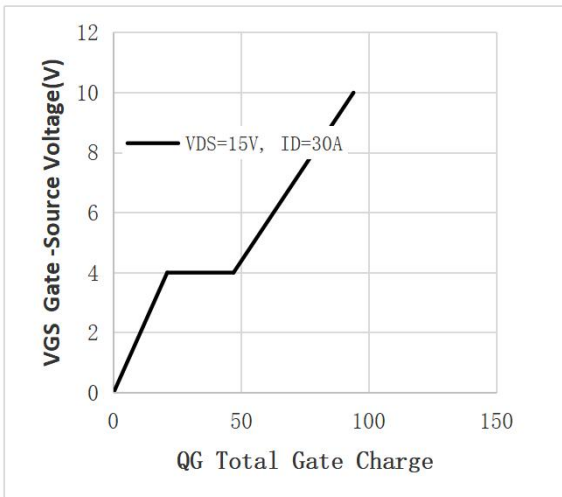


Fig.2 Capacitance Characteristics

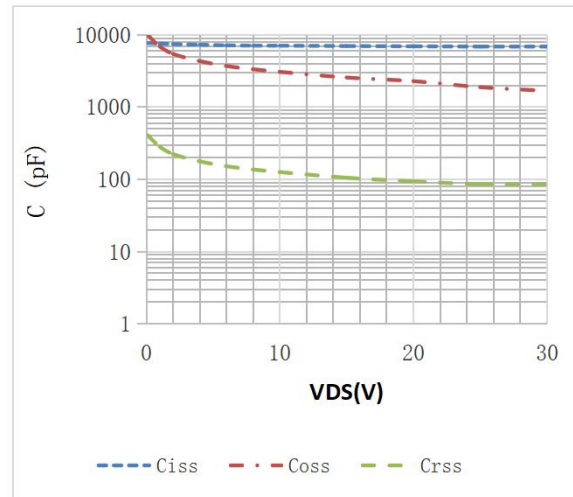


Fig.3 Power Dissipation

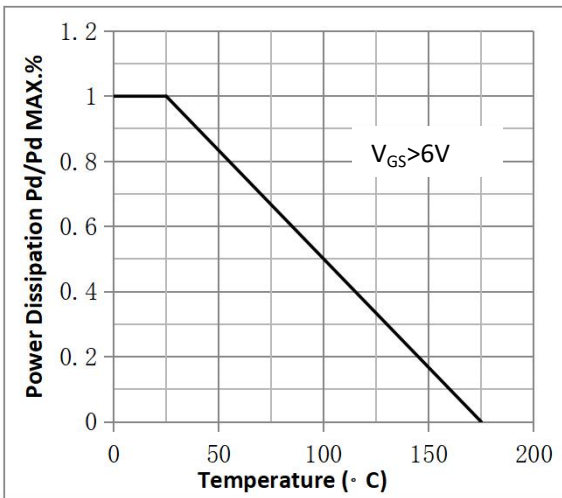


Fig.4 Typical output Characteristics

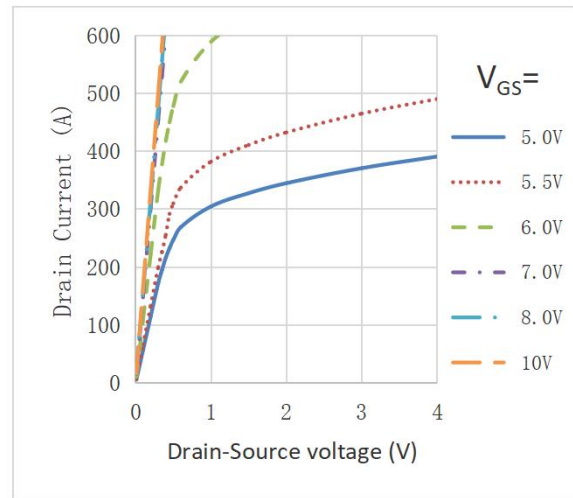


Fig.5 Threshold Voltage V.S Junction Temperature

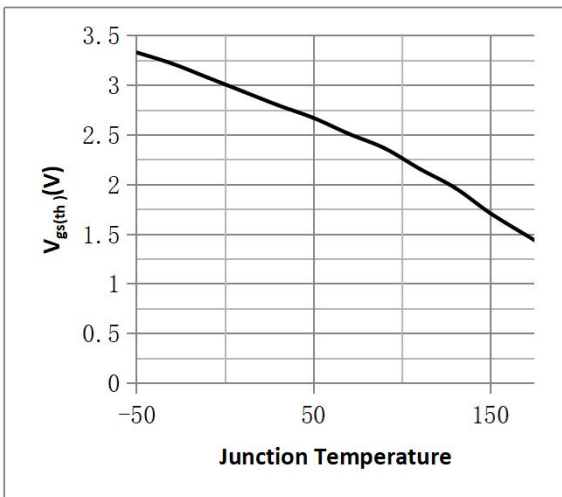


Fig.6 Resistance V.S Drain Current

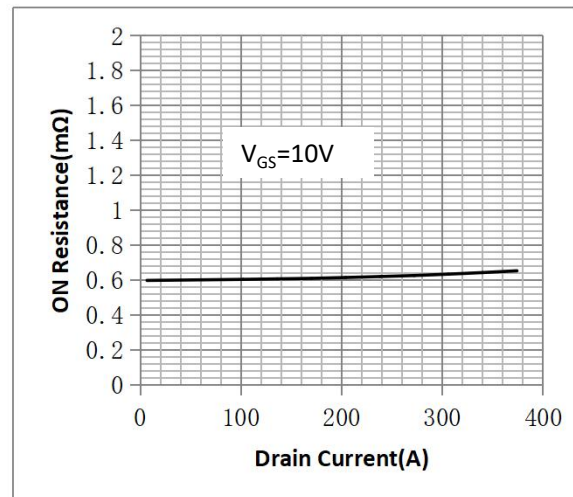


Fig.7 On-Resistance VS Gate Source Voltage

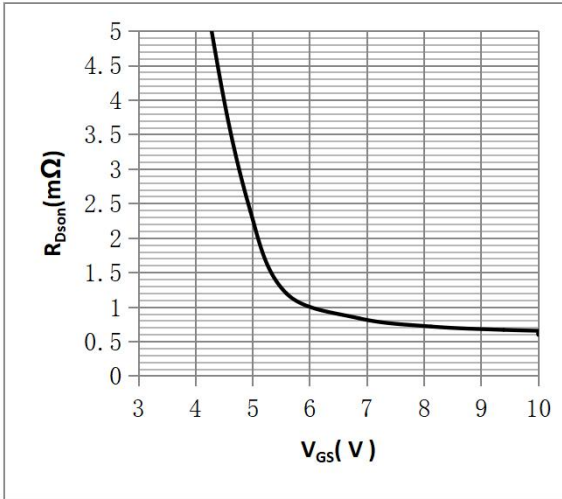


Fig.8 On-Resistance V.S Junction Temperature

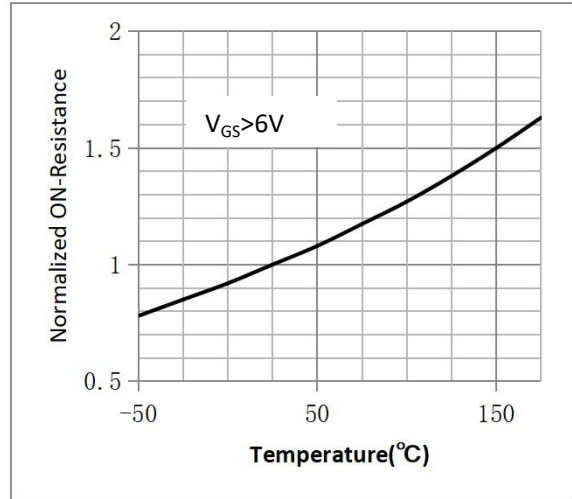


Figure 9. Diode Forward Voltage vs. Current

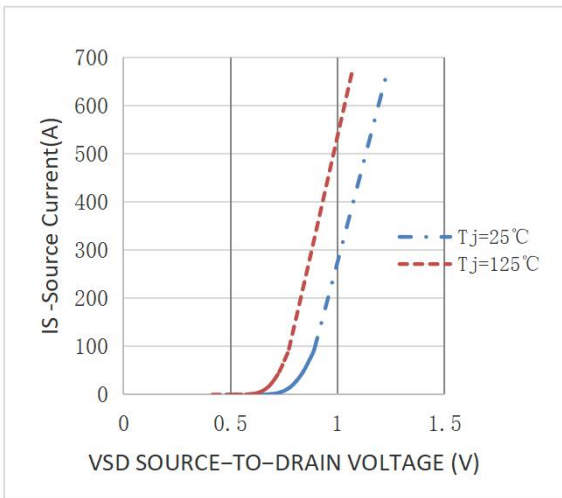


Figure 10. Transfer Characteristics

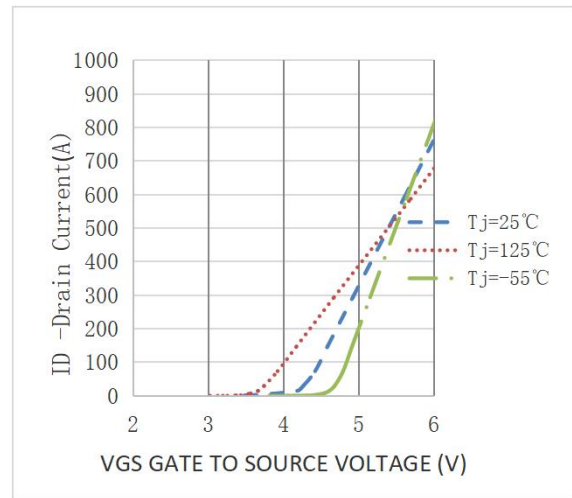


Fig.11 Safe Operating Area

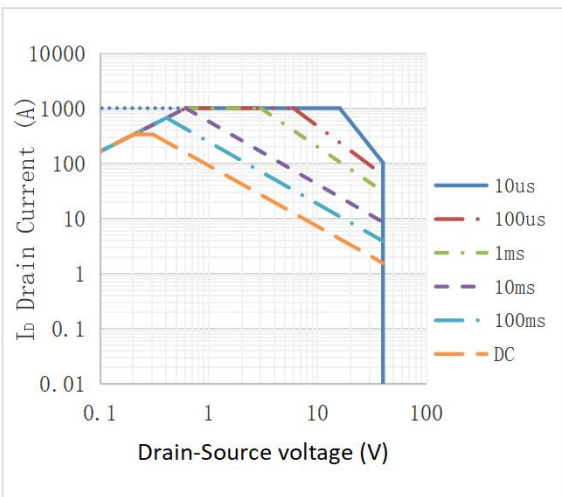
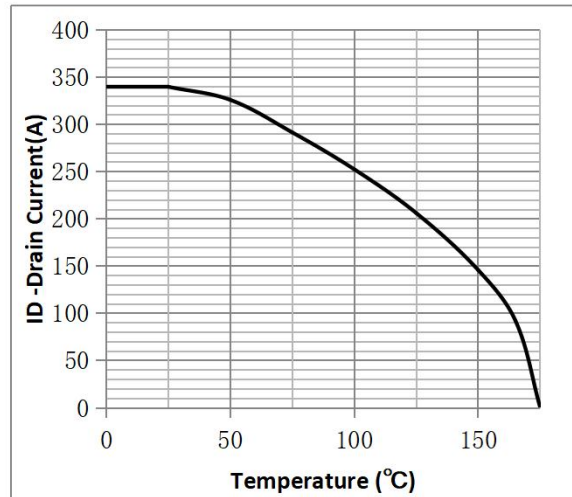
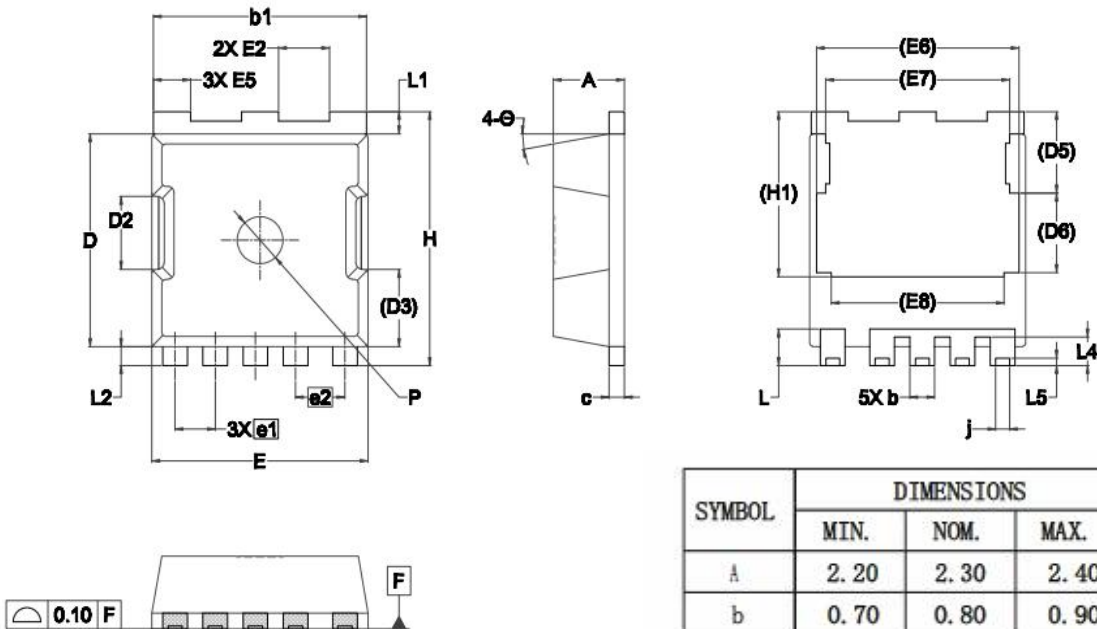


Fig.12 I_D vs. Case Temperature^③



•STOLL Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	6.80	6.90	7.00
c	0.40	0.50	0.60
D	6.60	6.70	6.80
D2	2.20	2.30	2.40
D3	2.43REF.		
D5	2.57REF.		
D6	2.50REF.		
E	6.90	7.00	7.10
E2	1.55	1.65	1.75
E5	1.10	1.20	1.30
E6	6.56REF.		
E7	5.96REF.		
E8	5.60REF.		
e1	1.20	1.30	1.40
e2	1.50	1.60	1.70
H	7.80	8.00	8.20
H1	5.20REF.		
L	1.05	1.15	1.25
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L4	0.80	0.90	1.00
L5	0.135	0.235	0.335
j	0.42	0.45	0.50
P	1.40	1.50	1.60
e	8.50*	—	11.50*

Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^\circ C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^\circ C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2024.1.10	NEW
B	2024.4.16	Modified ciss,Qg,switch time